CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

1. An analog front end for a digital subscriber line data communication system, comprising:

a line driver for transmitting a data signal over a local loop;

a digital to analog converter having an output connected to an input of the line driver, the digital to analog converter also having a data input for receiving a digital data signal and a clock input for receiving a clock signal; and

a data signal supervisor circuit having a first input configured to receive the data signal and a second input configured to receive the clock signal, the supervisor circuit having comparison circuitry for logically comparing a first value of the data signal in relation to a signal change of the clock signal to a second value of the data signal in relation to a previous signal change of the clock signal and asserting a transmit control output signal if the first value of data signal is the same as the second value of the data signal.

2. The analog front end of claim 1, further comprising:

a clock detector circuit having an input configured to receive the clock signal, the clock detector circuit further including frequency detection circuitry configured to assert a reset signal in response to the frequency of the clock signal.

3. The analog front end of claim 1, further comprising:

a control circuit having a reset input configured to receive a reset signal from the clock detector, the control circuit configured to reinitialize the digital subscriber line data communication system in response to the reset signal.

4. The analog front end of claim 3, wherein the control circuit includes circuitry for commanding the digital to analog converter to disable an output signal.

5. The analog front end of claim 1, wherein the comparison circuitry includes a counter circuit configured to count a predetermined number of clock signal cycles wherein the data signal remains unchanged.

6. The analog front end of claim 5, wherein the comparison circuitry further comprises Exclusive Or logic having an input that is indicative of the logical comparison of a first value of the data signal with a second value of the data signal, the Exclusive Or logic being in communication with an input of the counter circuit.

7. An analog front end for a digital subscriber line data communication system, comprising:

means for transmitting a data signal;

means for converting a digital input signal into an analog representation of the digital input signal;

means for detecting an at least one data signal anomalous condition; and

means for asserting an at least one transmit control output signal in response to the at least one data signal anomalous condition.

8. The analog front end of claim 7, wherein the means for transmitting a data signal receives a digital data stream from a delta-sigma modulator.

9. The analog front end of claim 7, wherein the means for detecting an at least one data signal anomalous condition is performed by monitoring a digital data stream.

10. The analog front end of claim 9, wherein the digital data stream comprises a data signal and a clock signal.

11. The analog front end of claim 10, wherein the means for detecting an at least one data signal anomalous condition is performed by a data supervisor.

12. The analog front end of claim 10, wherein the means for detecting an at least one data signal anomalous condition is performed by a clock detector.

13. A method for monitoring data transmissions in an analog front end, comprising:

comparing consecutive values of a digital data signal in relation to a clock signal; and

identifying a transmission error condition if there is no substantial change in the consecutive values of the digital data signal within a predetermined number of clock signal cycles.

14. The method of claim 13, further comprising:

monitoring the frequency of the clock signal; and

generating a reset signal if the frequency of the clock signal falls below a predetermined value.

15. A transmission signal integrity supervisor, comprising:

a clock detector configured to receive a clock signal input and generate a first output signal in response to an at least one clock signal input anomalous condition; and

a data supervisor configured to receive a digital data stream and generate a second output signal in response to an at least one digital data stream anomalous condition.

16. The signal integrity supervisor of claim 15, wherein the first output signal is a reset signal.

17. The signal integrity supervisor of claim 15, wherein the second output signal is a power down signal.

18. The signal integrity supervisor of claim 15, wherein the data supervisor receives a digital data stream from a delta-sigma modulator.

19. The signal integrity supervisor of claim 15, wherein the clock detector comprises a first monostable circuit and a second monstable circuit.

20. The signal integrity supervisor of claim 19, wherein the clock detector further comprises:

a current mirror; and

a resistor – capacitor combination having a resistance and a capacitance value respectively, selected such that the first output signal triggers in response to a clock signal input that falls below a minimum frequency.

21. The signal integrity supervisor of claim 15, wherein the data supervisor comprises:

a comparator; and

a maximum number counter.

22. The signal integrity supervisor of claim 21, wherein the comparator is configured to compare a data value from a previous clock cycle with a current data value and to generate a reset signal in response to consecutive data levels that vary.

23. The signal integrity supervisor of claim 21, wherein the maximum number counter is configured to increment upon detecting a clock cycle until it receives the reset signal from the comparator.

24. The signal integrity supervisor of claim 23, wherein the maximum number counter is configured to generate an output signal upon reaching a maximum count.

25. The signal integrity supervisor of claim 24, wherein the maximum number counter comprises a 4-bit asynchronous counter.

26. A circuit, comprising:

means for monitoring a digital data stream; and

means for generating an output signal in response to an anomalous condition in the digital data stream.

27. The circuit of claim 26, wherein the anomalous condition in the digital data stream would create a direct current (DC) transmit signal.

28. The circuit of claim 26, wherein the means for monitoring a digital data stream comprises a signal integrity supervisor.

29. The circuit of claim 28, wherein the signal integrity supervisor comprises a clock detector and a data supervisor.

30. The circuit of claim 28, wherein the means for generating an output signal is responsive to a digital data stream having a number of consecutive data values of equal magnitude wherein the number of consecutive data values reaches a predetermined maximum value.

31. The circuit of claim 28, wherein the means for generating an output signal is responsive to a digital data stream having a clock signal that falls below a predetermined minimum frequency.

32. A transmission unit, comprising:

a signal integrity supervisor configured to generate a response to a digital data stream having an anomalous condition.

33. The transmission unit of claim 32, wherein the digital data stream anomalous condition is a clock signal frequency that falls below a predetermined minimum value.

34. The transmission unit of claim 32, wherein the digital data stream anomalous condition is a data signal having a corresponding data value that does not vary for a predetermined maximum number of clock cycles.

35. A method for preventing a transmission unit from forwarding a transmit signal that may result in a DC flow condition, comprising:

monitoring a data signal;

generating a first signal in response to a data signal condition;

monitoring a clock signal; and

generating a second signal in response to clock signal condition.

36. The method of claim 35, wherein the data signal is provided by a delta-sigma modulator.

37. The method of claim 35, wherein the step of monitoring a data signal is performed with a digital comparator.

38. The method of claim 35, wherein the first signal is a power down signal.

39. The method of claim 38, wherein the power down signal is generated in response to a data signal having an unchanging value.

40. The method of claim 39, wherein the power down signal is generated by an asynchronous counter that reaches a maximum value.

41. The method of claim 35, wherein the second signal is a reset signal.

42. The method of claim 41, wherein the reset signal is generated in response to a clock signal having a frequency that fails to exceed a predetermined minimum value.

43. The method of claim 42, wherein the reset signal is generated by a monostable circuit.